

IN THE CLAIMS

Please amend the claims as follows:

Claims 1-26 (Canceled).

Claim 27 (Currently Amended). ~~Sealing processing for two wafers~~ A method of sealing a first wafer and a second wafer each made of semiconducting materials, comprising:

~~a step for implantation of implanting a metallic species in at least the first wafer,~~  
~~a step for assembly of assembling the first wafer and the second wafer by molecular bonding, and~~

~~a step for formation of after the molecular bonding, forming a metallic compounds, alloys~~ ohmic contact including alloys formed between the implanted metallic species and the semiconducting materials of the two wafers ~~first wafer and the second wafer, said metallic compound forming a resistive contact between the two wafers, at the metallic ohmic contact being formed at an assembly interface between the first wafer and the second wafer,~~  
wherein the forming includes causing the implanted metallic species to diffuse towards the interface between the first wafer with the second wafer and beyond the interface.

Claim 28 (Currently Amended). ~~Process~~ The method according to claim 27, wherein the formation step of the metallic compounds resulting from forming includes applying a heat treatment at a temperature equal at least to the a formation temperature of the said alloys compounds.

Claim 29 (Currently Amended). ~~Process~~ The method according to claim 27, wherein the implanting includes implanting the metallic species being implanted at a depth ( $R_p$ ) of

between 5 nm and 20 nm under ~~the~~ a surface of the implanted ~~first~~ wafer.

Claim 30 (Currently Amended). ~~Process~~ The method according to claim 27, wherein the implanting includes implanting the metallic species being implanted at a dose of between  $10^{14}$  and ~~a few~~  $10^{18}$  species/cm<sup>2</sup>.

Claim 31 (Currently Amended). ~~Process~~ The method according to claim 27, also further comprising:

~~an amorphisation step before assembly processing the first wafer~~ to make all or part of the a surface layer of the first wafer amorphous.

Claim 32 (Currently Amended). ~~Process~~ The method according to claim 31, wherein the amorphisation step comprising deposition of ~~processing includes depositing~~ an amorphous material layer before and/or after implantation of the metallic species.

Claim 33 (Currently Amended). ~~Process~~ The method according to claim 31, wherein the amorphisation step comprising a surface implantation, for example by ~~processing includes~~ implanting hydrogen or metallic species.

Claim 34 (Currently Amended). ~~Process~~ The method according to claim 27, each of the wafers being wherein the first wafer and the second wafer are made from a material chosen from among silicon, gallium arsenide (GaAs), SiC (silicon carbide), InP (Indium phosphide), Germanium (Ge), or [[le]] silicon-Germanium (SiGe).

Claim 35 (Currently Amended). ~~Process-~~The method according to claim 27, wherein the implanted species ~~being~~includes one or more of Nickel, and/or palladium, and/or Cobalt, and/or Platinum, and/or Tantalum, and/or Tungsten, and/or Titanium, and/or or Copper.

Claim 36 (Currently Amended). ~~Process-~~The method according to claim 27, wherein at least one of the wafers ~~being~~is a heterostructure, for example of the SOI type.

Claim 37 (Currently Amended). ~~Process-~~The method according to claim 27, further comprising:

thinning at least one of the wafers ~~being thinned~~, after assembly ~~the assembling~~ or after the ~~formation step~~forming of ~~the~~ metallic compounds.

Claim 38 (Currently Amended). ~~Process-~~The method according to claim 27, wherein at least one of the wafers ~~being~~is a debondable structure.

Claim 39 (Currently Amended). ~~Process-~~The method according to claim 27, wherein at least one of the wafers ~~comprising~~includes a weakening plane.

Claim 40 (Currently Amended). ~~Process-~~The method according to claim [[27]] 39, further comprising:

thinning the wafer ~~comprising a~~including the weakening plane ~~being thinned by~~ fracture along ~~the said~~ weakening plane, after assembly ~~the assembling~~ or after the ~~formation~~ ~~step~~forming of the metallic compounds.

Claim 41 (Currently Amended). ~~Process~~ The method according to claim 27, wherein at least one of the wafers ~~comprising~~ includes at least one circuit or ~~circuits~~ circuit layer, ~~on~~ ~~or close to its face to be assembled~~.

Claim 42 (Currently Amended). ~~Process~~ The method according to claim 27, wherein the ~~implantation step of metallic species being done through~~ implanting includes using a mask to obtain local implantation zones.

Claim 43 (Currently Amended). ~~Process~~ The method according to claim 27, also further comprising:

~~the formation of~~ forming an insulating layer on the first wafer, before it is implanted with metallic species the implanting.

Claim 44 (Currently Amended). ~~Process~~ The method according to claim 27, also further comprising:

[a] thinning ~~step of the implanted~~ first wafer after implantation of the metallic species.

Claim 45 (Currently Amended). ~~Process~~ The method according to claim 27, wherein the first wafer ~~comprising~~ includes at least one insulating zone located at ~~the~~ a surface so as to obtain local implantation zones.

Claims 46-52 (Canceled).

Claim 53 (Currently Amended). ~~Sealing processing for two wafers~~ A method of sealing a first wafer and a second wafer each made of semiconducting materials, comprising:

~~a step for implantation of implanting a metallic species in at least the first wafer, at a depth ( $R_p$ ) of between 5 nm and 20 nm under the a surface of said first wafer, at a dose of between  $10^{14}$  and a few  $10^{18}$  species/cm<sup>2</sup>,~~

~~a step for assembly of assembling the first wafer and the second wafer by molecular bonding,~~

~~a step for formation of after the molecular bonding, forming a metallic compounds, alloys ohmic contact including alloys formed between the implanted metallic species and the semiconducting materials of the two wafers first wafer and the second wafer, said metallic ohmic contact being disposed at compound forming a resistive contact between the two wafers, at the an assembly interface between the first wafer and the second wafer,~~

~~wherein the forming includes causing the implanted metallic species to diffuse towards the interface between the first wafer with the second wafer and beyond the interface.~~

Claim 54 (Currently Amended). ~~Process~~ The method according to claim 53, the formation step of the metallic compounds resulting from ~~wherein the forming includes applying a heat treatment at a temperature equal at least to the a formation temperature of the said metallic compounds.~~

Claim 55 (Currently Amended). ~~Process~~ The method according to claim 53, also further comprising:

~~-an amorphisation step before assembly processing the first wafer to make all or part of the a surface layer of the first wafer amorphous.~~

Claim 56 (Currently Amended). ~~Process~~ The method according to claim 55, wherein the amorphisation step comprising processing further comprises depositing deposition of an amorphous material layer before and/or after implantation of the metallic species.

Claim 57 (Currently Amended). ~~Process~~ The method according to claim 55, wherein the amorphisation step comprising processing includes implanting a surface implantation, for example by hydrogen or metallic species.

Claim 58 (Currently Amended): ~~Structure~~ A structure obtained by a process according to the method of claim 27, wherein the comprising two substrates made of semiconducting materials assembled by molecular bonding and having localised zones of metallic compounds at the assembly interface, these metallic compounds being alloys made from semiconducting materials of substrates at the assembly interface and include at least one metal chosen from among nickel, palladium, cobalt, platinum, tantalum, titanium, or copper.

Claim 59 (Currently Amended): ~~Structure~~ The structure according to claim 58, wherein the semiconducting materials being chosen are selected from among Si, GaAs, SiC, InP, or SiGe.

Claim 60 (Currently Amended): ~~Structure~~ The structure according to claim 58, wherein at least one of the substrates being is a heterostructure.

Claim 61 (Currently Amended): ~~Structure~~ The structure according to claim 58, wherein at least one of the substrates being is a thin film.

Claim 62 (Currently Amended): ~~Structure~~ The structure according to claim 58,  
wherein at least one of the substrates comprising includes one or more of electronic, and/or  
optical, or and/or-mechanical components.

Claim 63 (Currently Amended): ~~Structure~~ The structure according to claim 58,  
wherein one of the substrates being is a thin film made of silicon comprising RF circuits.

Claim 64 (Currently Amended): ~~Structure~~ The structure according to claim 63,  
wherein the other substrate being is made of high resistivity silicon.